REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Claim 7 is amended, Claims 12-19 are added, and Claims 1-19 are pending in the application.

The indication of informalities in claim 7 is acknowledged. It is believed that claim 7 has amended is in proper form.

Claims 1, 6, 7 and 11 stand rejected under 35 USC §103 in view of U.S. Patent No. 5,383,117 to Tateishi in view of U.S. Patent No. 6,347,395 to Payne et al. This rejection is respectfully traversed.

Each of the independent claims 1 and 7 specify testing a network switch chip, having an expansion port, by receiving an expansion port frame from the expansion port, and generating a new expansion port frame, and outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip.

Hence, the new expansion port frame is output to the expansion port of the network switch chip being tested.

Applicant traverses the Examiner's tortured interpretation of Tateishi et al: the Examiner asserts that the claimed network switch chip under test is taught by the packet switching testing apparatus 1a and the claimed external logic unit is taught Tateishi et al by the under-test device 6:

> *(See figure 1: block 6 (external logic unit), blocks 2a and 3a (expansion port)* [of the packet switching testing apparatus 1a] ... *the transmitting section transmits packet data to the under-test-device (hence receiving by the external logic unit)* ....
>
> (Page 2, sec. 3) (italics in original).

However, Tateishi et al. explicitly discloses that the "packet switching testing apparatus 1a tests the under-test device 6" and that "[t]he packet switching testing apparatus 1a includes a transmitting section 2a and a receiving section 3a." (Col. 6, lines 50-53).

Hence, in Tateishi et al. it is the transmitting section 2a of the packet switching testing apparatus 1a that transmits the packet data to the under-test device 6. Hence, Tateishi et al. teaches that received packet data is modified by the under-test device 6, as opposed to independent claims 1 and 7 which specify that the expansion port frame output from the expansion port of the network switch chip being tested is used to generate a new expansion port frame by the external logic unit based on reception of the expansion port frame.

Hence, the claims specify that the network switch chip under test outputs the expansion port frame, and the external logic generates the new expansion port frame based on reception of the expansion port frame. Any other interpretation would be inconsistent with the interpretation that those skilled in the art would reach, and hence would be unreasonable. Cf. In re Cortright, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

Hence, Tateishi et al. merely discloses that the testing apparatus 1a outputs the initial frame data and receives the modified frame data from the device under test, and the such performs the opposite of the features specified and claims 1 and 7.

Further, Tateishi et al. neither discloses no suggests an expansion port or an expansion bus, as claimed. Rather, Tateishi et al. discloses a plurality of input highways (IW1 through IWn) and a plurality of output highways (OW1 through OWn): there is no disclosure or suggestion that the disclosed "highway" is in any way equivalent to the claimed expansion port

of the network switch chip. In fact, Tateishi et al. provides absolutely no reference whatsoever to either the terms "expansion" or "port", let alone the claimed "expansion port".

The Official Action admits that Tateishi et al. fails to explicitly disclose a network switching chip configured for transferring data, and relies on Payne et al. for the teaching of a network switching chip. However, the hypothetical combination neither discloses nor suggests the claimed feature of the external logic unit generating a new expansion port frame based on reception of the expansion port frame, and outputting the new expansion port frame onto the expansion bus for reception by the expansion port of the network switch chip, as claimed.

For these and other reasons, the §103 rejection of claims 1, 6, 7, and 11 should be withdrawn.

Claims 2-5 and 8-10 stand rejected under 35 USC §103 in view of Tateishi et al., Payne et al., and further in view of U.S. Patent No. 5,721,728 to Fowler et al. This rejection is respectfully traversed.

One having ordinary skill in the art would not have been motivated to modify the hypothetical combination of Tateishi et al. and Payne et al. to include the teachings of Fowler et al. As admitted in the Official Action, "the application layer 14c generates a second user portion based on the test parameters", thereby precluding performing the steps within the claimed external logic unit -- rather, the application layer 14 is a software based procedure that is executed by a central processing unit, as opposed to implementation in a logic unit, as claimed.

For these and other reasons, the rejection of claims 2-5 and 8-10 should be withdrawn.

In view of the above, it is believed this application is and condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-360, and please credit any excess fees to such deposit account.

Respectfully submitted,

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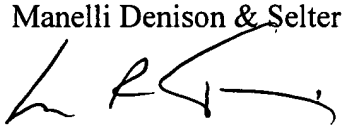

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